# Microinstruction Tables with Extended Control Signals

# Instruction: AND

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: ADD

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: LDA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: STA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: BUN

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: BSA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: ISZ

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: CLA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: CLE

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: CME

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: CMA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: CIR

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: CIL

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: INC

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: SPA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: SNA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: SZA

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: SZE

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Instruction: HLT

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Micro-Operation | MemWrite | s2s1s0 | LD AR | LD PC | LD DR | LD IR | LD AC | LD TR | Alu op | CLR AR | CLR PC | CLR DR | CLR AC | CLR TR | INC AR | INC PC | INC DR | INC AC | INC TR |
| D0T0: AR ← PC | 0 | 010 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T1: IR ← M[AR], PC ← PC + 1 | 0 | 111 | 0 | 1 | 0 | 1 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| D0T2: AR ← IR(11:0), IR ← IR(15) | 0 | 101 | 1 | 0 | 0 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T3: DR ← M[AR] | 0 | 111 | 0 | 0 | 1 | 0 | 0 | 0 | 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D0T4: AC ← AC ∧ DR, SC ← 0 | 0 | 000 | 0 | 0 | 0 | 0 | 1 | 0 | 0001 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |